Design and Performance Analysis of Heterojunction Dual Wire Gate All Around Nanosheet Field Effect Transistor

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Abstract

In this paper, we introduce a new variation of the Gate All Around Nanosheet Field Effect Transistor (GAA NS FET) called the Dual Wire (DW), which integrates source heterojunctions and strained channels. We assess its electrical properties across different temperatures (300K, 400K, and 500K) and compare them to those of the Heterojunction DW Gate All Around Nanosheet Field Effect Transistor (Heterojunction DW GAA NS FET) and the Conventional DW Gate All Around Nanosheet Field Effect Transistor (Conventional DW GAA NS FET). Our investigation encompasses the electrostatic control effects on DC and analog parameters, including gate capacitance (C_{GG}), transconductance (F_T), and cut-off frequency (F_T) for all three device types. The channel regions in our structures feature Silicon Germanium (SiGe) (Si/Ge/Si), and the introduction of strain and a heterojunction structure notably enhances device performance. To analyze the semiconductor device accurately, we solve the Density Gradient (DG) equation self-consistently, utilizing the Shockley-Read-Hall (SRH) equation to estimate carrier generation, considering bandgap narrowing in transport behavior, and accounting for auger recombination. Additionally, at temperatures of 300K, 400K, and 500K, the Heterojunction DW GAA NS FET exhibits substantial improvement in Ion and Ioff compared to the Conventional DW GAA NS FET. Overall, our results show a notable improvement in drain current, transconductance, and unity-gain frequency, with enhancements of around 34%, 9.5%, and 30%, respectively, observed across different temperatures. This improvement translates into superior RF performance for the Heterojunction DW GAA NS FET when compared to the conventional DW GAA NS FET.

Keywords: Half Heusler; Phase transition; dielectic function; Semiconductor; Bulk modulus; Band gap

1. Introduction

In recent decades, the semiconductor industry has seen significant progress aimed at enhancing the functionality of semiconductor devices. This progress has been driven by a continuous reduction in device size, resulting in increased transistor integration on a single chip and consequent improvements in device performance. This trend, illustrated by Moore's Law, predicts a doubling of transistors approximately every eighteen months [1-3]. The primary impetus for CMOS transistor miniaturization is to achieve increased density, improved speed, cost reduction, and superior performance in integrated circuit (IC) applications. However, this pursuit comes with a drawback: significant downsizing results in adverse short-channel effects (SCEs) and notable second-order consequences that impede technological progress. To address these challenges, the adoption of multi-gate transistors emerges as a promising strategy for future technological phases [4]. In successive technological advancements, device size has diminished, with each new stage witnessing a reduction in channel length, reaching dimensions at the atomic level. As the channel length decreases, the gap between the source and drain narrows, bringing them into very close proximity [5]. Over time, various alternative structures like Fin FET and gate-all-around (GAA) transistors have surfaced. Additionally, alternative methods have been introduced, including the integration of novel approaches like strain engineering and the incorporation of new substances into the CMOS process, such as high-k dielectrics and metal gate electrodes with varying work functions [6].

However, as technology nodes have diminished to below 3 nm, the FinFET structure has faced limitations. Consequently, there is an increasing necessity to develop a device with a gate-all-around (GAA) design, surrounding the entire channel with a gate [7-8]. As researchers strive to strike a balance between the size of FETs and GAAs alongside contemporary technology, a

pivotal factor in enhancing device performance and achieving superior gate controllability, they are exploring Heterojunction Gate-All-Around Nanosheet FETs as potential candidates for upcoming logic devices [9]. The current pinnacle in semiconductor technology for manufacturing commercial logic devices is exemplified by Nanosheet Field-Effect Transistors (FETs). Its success is predominantly attributed to the heightened effective channel width and improved gate controllability compared to earlier FET models [10]. This innovative arrangement entails converting the wire-like channel structure into a nanosheet, thereby maximizing the contact area between the channel and the gate.

Nanosheet field effect transistors (NS FETs) are emerging as a promising transistor technology for future analog/RF System-on-Chip (SoC) applications in the 3 nm technology era. Their ability to reduce gate length (LG) enhances performance at lower operating voltages and increases chip density [11-13]. Numerous studies have explored various nanoscale transistor designs, primarily focusing on their application in low-power scenarios to mitigate short-channel effects [14]. The gate-all-around (GAA) design of nanosheet field-effect transistors (NSFETs) effectively controls nanosheet channels, addressing short-channel effects [15]. Meanwhile, NHJS technology enables digital CMOS scaling through FinFET and multi-gate techniques, providing a foundation for outstanding analog and radio frequency (RF) integration capabilities [16].

In 2018, Chu at al introduced a significant development by creating a horizontally layered p-type Ge-NSFET through a low-pressure chemical vapor deposition (LPCVD) technique [10]. The formation of drain and source contacts remains a crucial challenge during the construction of vertically stacked GAA NSFETs [17]. Sooner, Y. S. Huang and colleagues [12] conducted an experimental demonstration where they successfully manufactured p-type vertically stacked GAA NSFETs using GeSn materials and a chemical vapor deposition (CVD) process, incorporating three nanosheets [18].

Various materials, including InGaAs, Ge, Si, SiGe, and GeSn, have been employed as nanosheets in NSFET designs. Critical factors affecting the analog/RF performance of NSFETs encompass parameters such as gate length (L_G), nanosheet width (W_{NS}), gate metal work function, channel thickness, gate oxide permittivity, and gate dielectric thickness [19]. Over time, there has been a growing interest in exploring novel devices that propose advancements in architecture and material metallurgy. One effective channel engineering technique involves introducing strain and heterojunction structures on the Nanosheet field-effect transistor [20]. In this investigation, we present an innovative design for a Nanosheet Heterojunction GAA FET utilizing dual wires. We conducted a thorough 3D analysis of its DC and AC performance, comparing the results with the conventional structure, which serves as the focal point of our research. Within the proposed design, we successfully regulated the transistor's performance before fully activating the channel, employing dual wires (DW) at the extreme left and right ends of the channel. Our findings indicate that in both DC and AC assessments, the proposed structure outperforms the primary design. The remainder of this paper is structured as follows:

Section 2 provides details on the design, geometry, and simulation methods for the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET. Brief discussions regarding potential applications for the proposed device are presented. In Section 3, we delve into the influences of strain engineering and the heterojunction structure on the electrical characteristics and analog/RF parameters of the devices. Finally, Section 4 summarizes our key findings.

2.Device structure and Simulation method

Certainly! Here is the revised text with grammatical corrections: In Fig. 1, schematic views of 3D structures for the Heterojunction DW GAA NS FET and the Conventional DW GAA NS FET are depicted, both featuring a rectangular cross-section. The Heterojunction DW GAA NS FET includes a germanium source [21], dual wire (DW) channels composed of silicon and germanium [22], and silicon for the drain. In contrast, the Conventional DW GAA NS FET employs silicon for the source and drain regions, with channels comprising SiGe [23-24]. Notably, tensile-strained SiGe plays a crucial role in altering energy levels within these structures [25].

In our simulations, a set of parameters for the Heterojunction DW GAA NS FET and the Conventional DW GAA NS FET was utilized, as summarized in Table 1. Aluminum metal with a 4.7 eV work function served as the gate, generating an internal electric field. This electric field repels electrons from the channel in the OFF state. The parameters include t_{si} (silicon body thickness), W (channel width), and L (channel length). We assumed a gate oxide thickness of 0.5 nm for SiO_2 and 1.5 nm for HfO_2. For a comprehensive understanding of material properties, please refer to Table 2. As depicted in Fig. 2, the transfer characteristics of the primary structure were compared to those of a reference transfer characteristics curve to calibrate the parameters used in the simulations.

To enhance the precision of our simulations, we adopted an effective quantum-corrected potential as the foundation for a Scharfetter-Gummel discretization scheme [26]. We subsequently solved these equations using the 3D ATLAS simulator [27]. To ensure accurate predictions of subthreshold performance and Auger recombination [28], our simulations incorporated the bandgap narrowing (BGN) model. Additionally, we utilized the Shockley-Read-Hall (SRH) model to evaluate carrier generation and recombination processes, aiding in forecasting the impact of doping on device characteristics. Furthermore, Fermi-Dirac (F-D) statistics were considered, outlining the probability of electrons or holes occupying specific energy levels in states of equilibrium [29]. As illustrated in Fig. 2, the transfer characteristics of the main structure were compared with the transfer characteristics curve in reference [23] to calibrate the parameters and models used in the simulations.

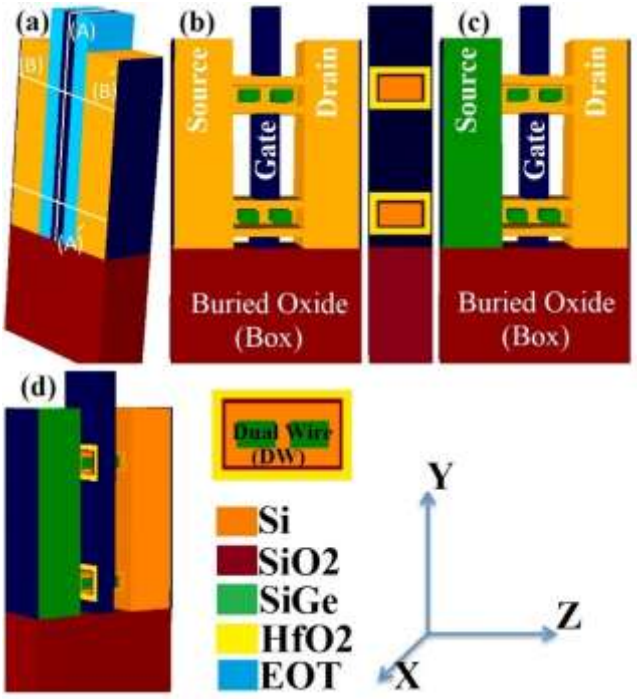


Fig. 1. (a)3D schematic view of Conventional DW GAA NS FET with nitride spacer (b) 2D view and cross section of Conventional DW GAA NS FET (c) cross section of Heterojunction DW GAA NS FET (d) 3D schematic view of Heterojunction DW GAA NS FET

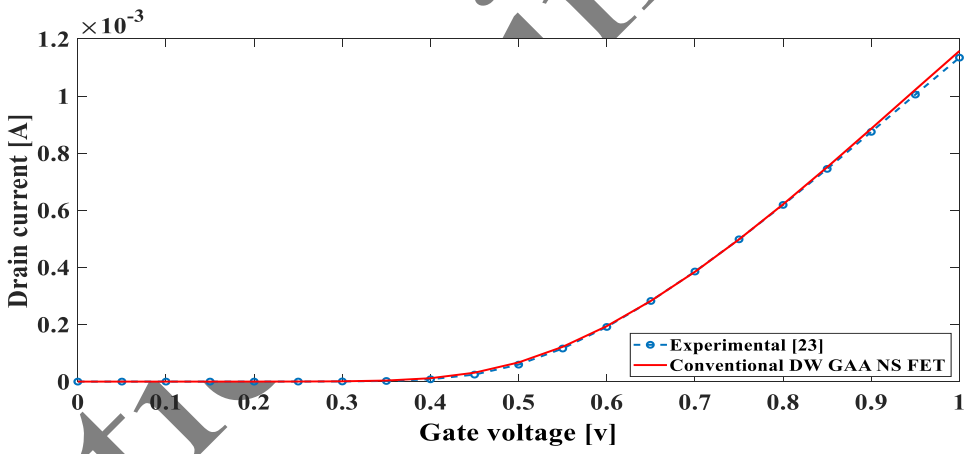


Fig. 2. Validation of the transfer characteristics curve obtained from simulation of Heterojunction DW GAA NS FET with the experimental data.

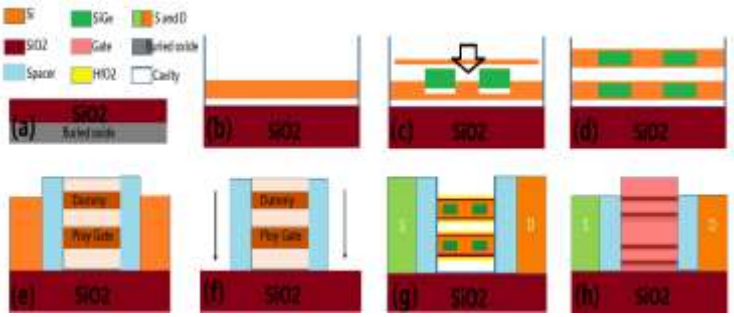


Fig. 3. Final steps of a possible process flow for the fabrication of Heterojunction DW GAA DW FET

Table 1: Parameters used for devices modeled in this work

	Heterojunction and Conventional DW GAA NS FET
Height of the devices (nm)	60
Height of the substrate (nm)	30
Channel material/height (nm)	Strained-Si/1.0+ Relaxed-SiGe/3.0 +Strained-Si/1.0
Source/Drain material	Heterojunctio DW GAA NS FET(Ge/Si) Conventional DW GAA NS FET(Si/Si)
Nanosheet width (nm)	15
Gate length(nm)	5
Source/Drain length (nm)	12
Channel doping	Without doping
Source/Drain doping	n.type 10^{20}
Dual wire doping	p.type 10^{16}
Comtent of Ge in $Si_{1-x}Ge_x$	X = 0.2
Dual Wire layer L/W/H (nm)	4/10/3
Spacer dielectric/Underlap (nm)	Nitride\5

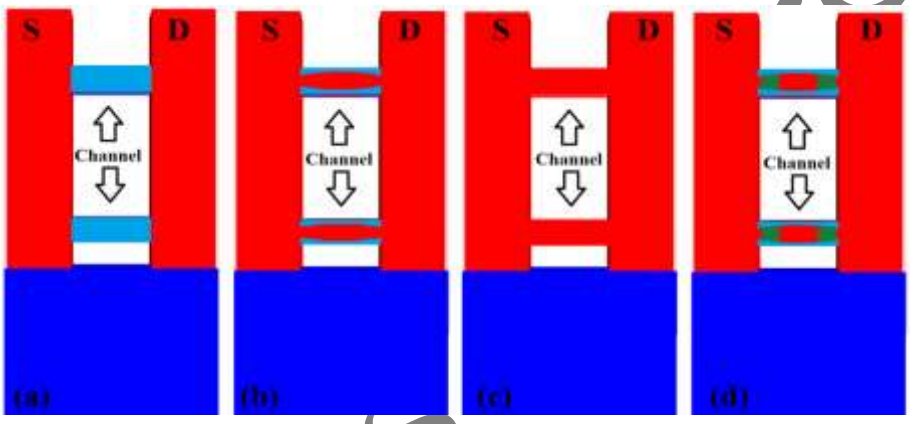


Fig. 4. Channel modes (a) Full depletion, (b) Partial depletion, (c) Accumulation, and (d) Blocked channel in the partial depletion mode by dual wire

Table 2: Material properties used in this work (x is the Ge content in the $Si_{1-x}Ge_x$) (24)

Parameter	Equation used
Electron affinity	$X_{Strained-Si} = 4 \cdot 05 + 0 \cdot 58x$ $X_{SiGe} = 4 \cdot 05 - 0 \cdot 05x$
Band gap energy	$E_{gStrained-Si} = 1 \cdot 12 - x(0 \cdot 31 + 0 \cdot 53x)$ $E_{gSiGe} = 1 \cdot 12 - 0 \cdot 42x$
Conduction band offset	$\Delta E_c = 0 \cdot 63x$
Valance band offset	$\Delta E_v = x(0 \cdot 74 - 0 \cdot 53x)$

Figure 3 (a to h) illustrates the eight sequential stages involved in producing the proposed device. As shown in Fig. 3, only one undoped wafer is required to create the device, and SOI technology is also a viable option. Initially, a layer of SiO_2 was applied to the Si wafer to form a buried oxide (BOX) (a), and then a layer of Si was added to the SiO_2 wafer to form the first channel (b). The subsequent step (c) involved etching dual wire spaces, with SiGe being deposited on both sides of the channels at specific locations. Importantly, when depositing SiGe into the channel, the other side of the channel must be masked. Following this, dual wire doping was carried out. In the third step of channel formation, a layer of silicon is deposited. The second channel is produced using the same procedure (d). Afterwards, spaces around the channels were filled with SiO_2 and high-k dielectrics (e). Fig. 3(g) demonstrates that after etching, source, drain, and gate metals were deposited on both sides at specific locations. Finally, Fig. 3(h) reveals the ultimate schematic of the device following the placement of the source and drain electrodes [30-31].

To articulate the core concept of this study accurately, we examined the positions of electrons and holes in the channel under the influence of the gate voltage. As illustrated in Fig. 4(a), in the OFF state of the transistor with no voltage applied to the gate, an internal electric field arises due to the disparity between the work functions of the gate metal and the semiconductor. This electric field results in the depletion of electrons in the center of the channel. When the voltage surpasses the threshold but remains below the flatband voltage, the channel transitions into a partial depletion mode,

illustrated in Fig. 4(b). Further elevation of the voltage, beyond the flatband voltage, fully opens the channel, entering the accumulation mode, as depicted in Fig. 4(c). The central concept of this paper, inspired by Fig. 4(b), is depicted in Fig. 4(d). By applying p-type doping with a concentration of 10^6 to the wires, the center of the channels are obstructed when the transistor is the partially depleted mode. As a result, if unintended voltages below the flatband voltage are applied to the gate, the current is minimized. Specifically, in this mode, the channel is blocked near the oxide surface, leaving only the center accessible. Therefore, wires with opposite doping were chosen instead of walls with opposite doping. To provide a deeper understanding of the proposed structure, the following sections will elaborate on the simulation results. Introducing opposite doping at specified points effectively blocks the center of the channel during the partially depleted mode of the transistor. As a result, when unintentional voltages lower than the flatband voltage are applied to the gate, the resulting current is minimized. In this partially depleted mode, the channel is blocked near the oxide surface, leaving only the central part open in this structure. Notably, wires featuring opposing doping were used instead of walls with differing doping profiles. To enhance understanding of the proposed structure, the subsequent section provides detailed insights into the simulation results. In the absence of channel doping, the initial investigation focused on the electron positioning in both structures.

Figure 5(a) illustrates the concentrations of electrons and holes in the Heterojunction DW structure compared to those in the Conventional DW structure during the OFF state along the AA' cutline. The figure shows that electrons in the channel of both structures are influenced by the internal electric field resulting from the difference in work functions between the gate metal and the semiconductor.

However, despite both structures sharing the same internal electric field and work function difference, more electrons are expelled from the channel in the Heterojunction DW structure compared to the Conventional DW structure. This phenomenon can be attributed to the Heterojunction DW structure, where holes are located closer to the center of the channel and are more susceptible to the influence of the electric field. Consequently, a higher concentration of holes is observed in the center of the channel, indicating that this structure achieves a more effective depletion state without requiring a significant difference in the work functions of the gate metal and the semiconductor. Given the accumulation of a greater number of holes in the center of the channel in the Heterojunction DW structure during the OFF state, band diagrams were also examined.

The energy band diagrams along the BB' cutline are illustrated in Fig. 5(b) in the OFF state. It is evident that in this state, the Fermi level is situated closer to the conduction band in the main structure when compared to the DW structure. This indicates that the channel of the DW structure has been depleted of more carriers in the OFF state.

Fig. 5(c) illustrate the energy bands in the ON state with $0 \cdot 6V$ applied to the drain terminal and $0\ to\ 1.0V$ applied to the gate terminal along the BB' cutline for Heterojunction DW GAA NS FET and Conventional DW GAA NS FET. In the ON state, at the center of the channel, it is evident that the conduction bands overlap for both Heterojunction DW GAA NS FET and Conventional DW GAA NS FET. This indicates that an equal amount of electrons accumulates in the middle of the channel in both structures.

3.Results and Discussions

3.1 DC Analysis

Fig. 6 illustrates the $I_D\_V_G$ characteristics under different temperature conditions. Notably, as the temperature decreases, the drain current (I_D) increase. This enhancement in I_D can be attributed to the improved mobility of charge carriers at the source-channel interface, as illustrated in Fig. 6(a) and 6(b). The electron mobility can be determined using a linear regression technique, as outlined in references [27] and [28]. The mobility can be inferred from the relationship between drain current and electron mobility in the transfer characteristics [28]. In particular, electron mobility can be calculated by taking the derivative of I_D with respect to drain voltage. Equations (1) to (4) demonstrate that electron mobility is directly linked to changes in drain current, indicating its sensitivity to the electric field.

$$I_D = \frac{\mu_{eff} C_{ox}}{2}\left(\frac{W}{L}\right)(2(V_{GS} - V_T)V_{DS} - V_{DS}^2) \quad (1)$$

If V_{DS} is low, then

$$I_D \cong \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_T)V_{DS}\right) \quad (2)$$

$$\frac{\partial I_D}{\partial V_{DS}}\Big|_{small V_{DS}} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T) \quad (3)$$

$$\mu_{eff} = \frac{\left(\partial I_D / \partial V_{DS}\right)\big|_{V_{DS}}}{C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)} \quad (4)$$

In the context of points (1) to (4), it's important to note that electron mobility correlates with variations in drain current. This implies that it can also be influenced by the electric field. The heterojunction structure and dual wire (DW) channels within the device's channel enhance the electric field strength beneath the gate region. Nevertheless, it is the "effective" electron mobility that is predominantly determined by the source and drain regions. Typically, the source and drain regions exhibit the lowest electron mobility due to their high doping levels. Furthermore, the presence of a heterojunction structure contributes to enhanced mobility at the interface between the source and channel.

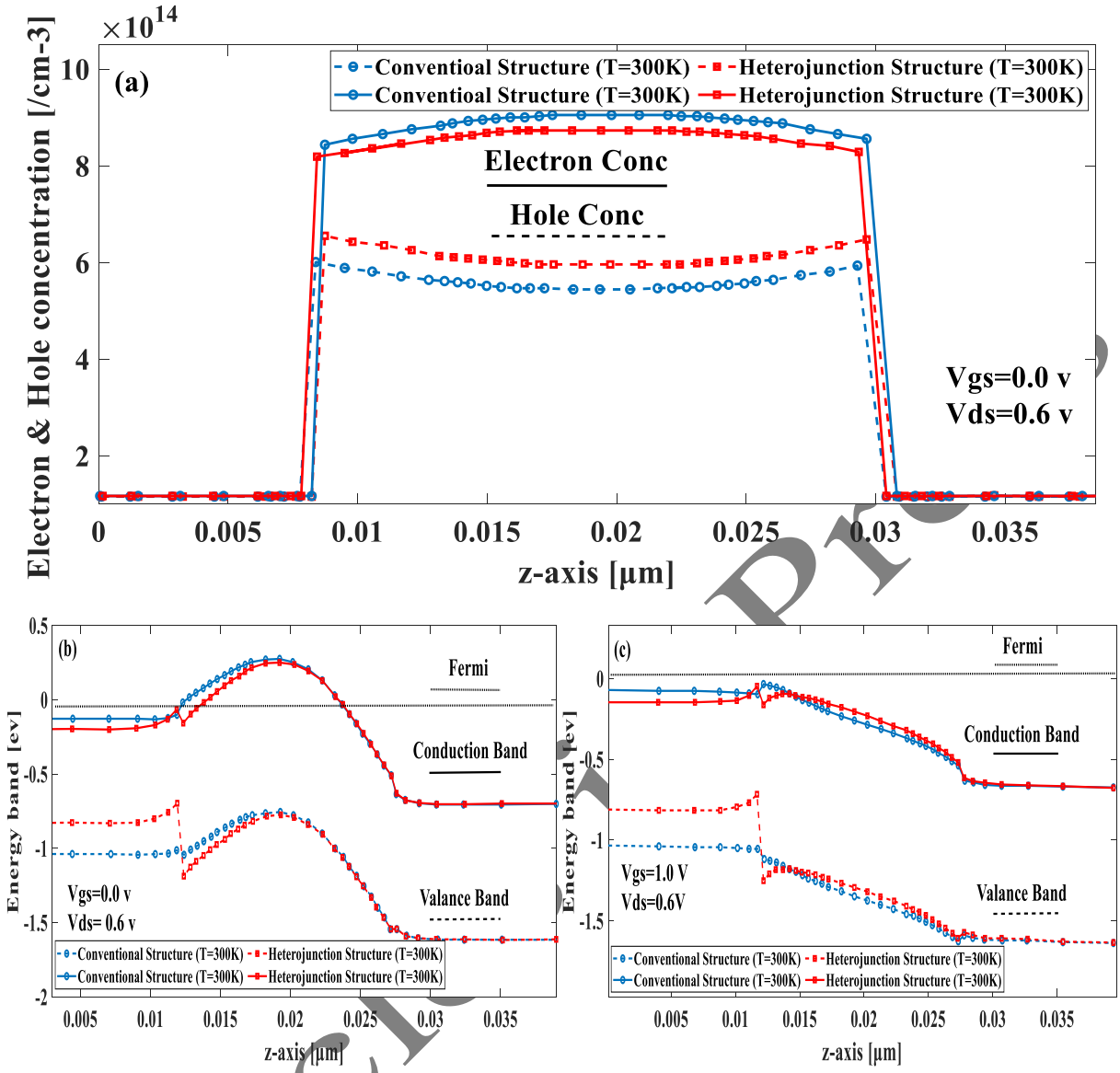


Fig. 5. (a) Electrons and holes concentration for the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET in the OFF state along the AA' cutline ($V_{DS} = 0 \cdot 6V$, and $V_{GS} = 0 \cdot 0V$), (b) Energy band diagrams for the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET in the OFF state along the BB' cutline ($V_{DS} = 0 \cdot 6V$, and $V_{GS} = 0 \cdot 0V$), (c) Energy band diagrams for the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET in the ON state along the BB' cutline ($V_{DS} = 0 \cdot 6V$, and $V_{GS} = 1 \cdot 0V$)

Table 3: Electrical characteristics of Heterojunction DW GAA NS FET and Conventional DW GAA NS FET

Devices (node)	Vth(v)	Ion(A)	Ioff(A)
CDWNs(300K)	$0 \cdot 299$	$1 \cdot 18 * 10^{-3}$	$1 \cdot 69 * 10^{-10}$
HDWNs(300K)	$0 \cdot 237$	$1 \cdot 71 * 10^{-3}$	$4 \cdot 79 * 10^{-10}$
CDWNs(400K)	$0 \cdot 217$	$0 \cdot 80 * 10^{-4}$	$8 \cdot 04 * 10^{-10}$
HDWNs(400K)	$0 \cdot 185$	$1 \cdot 20 * 10^{-4}$	$1 \cdot 76 * 10^{-8}$
CDWNs(500K)	$0 \cdot 144$	$6 \cdot 09 * 10^{-4}$	$8 \cdot 31 * 10^{-8}$
HDWNs(500K)	$0 \cdot 107$	$8 \cdot 85 * 10^{-4}$	$1 \cdot 56 * 10^{-7}$

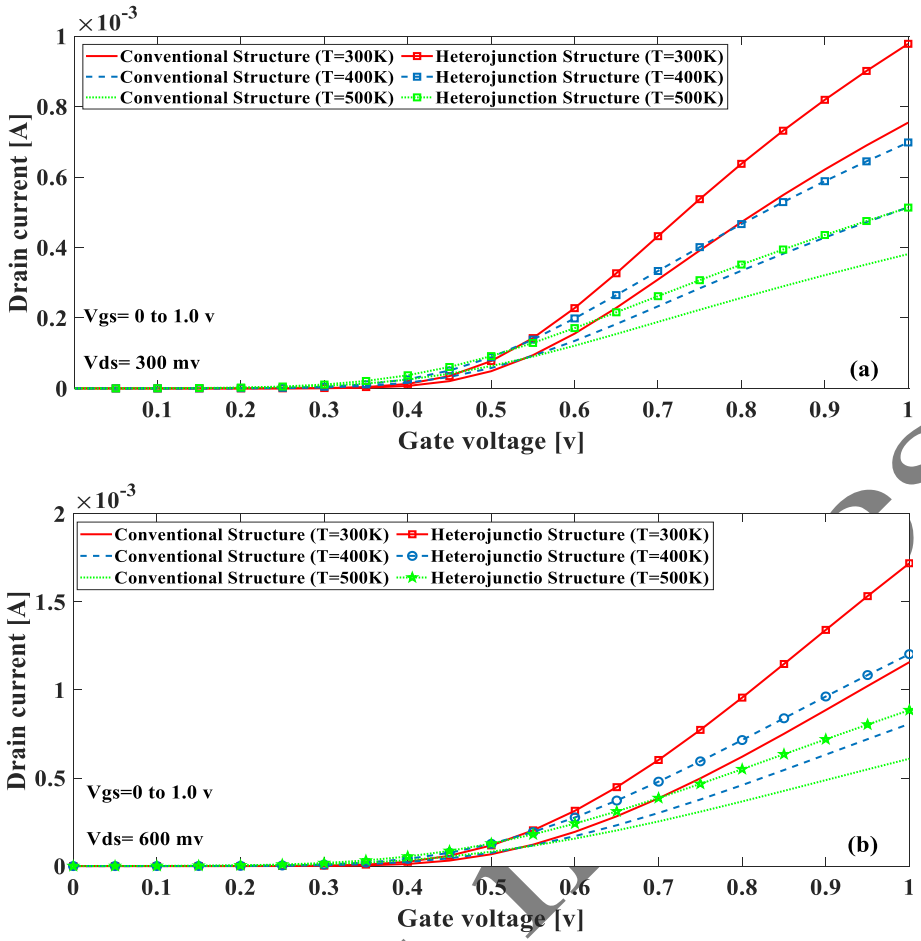


Fig. 6. Drain current of the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET under versus gate voltage at temperatures of 300 K, 400 K, and 500 K, (a) $V_{DS} = 0 \cdot 3V$, (b) $V_{DS} = 0 \cdot 6V$

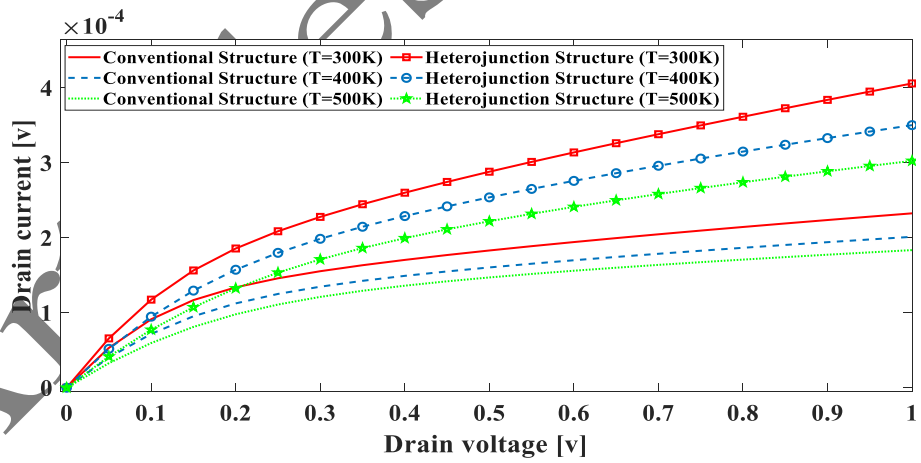


Fig. 7. Drain current of the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET under versus drain voltage at temperatures of 300 K, 400 K, and 500 K

In Fig. 7, we illustrate the changes in drain current for both Heterojunction DW structures and Conventional DW GAA NS FET at varying temperatures (300K, 400K, and 500K), depicting them as functions of drain voltage under different V_{GS} conditions. When a drain voltage is applied, it propels charge carriers through the transistor's channel region. Higher temperatures result in the breaking of silicon lattice bonds, leading to the creation of electron-hole pairs and an increased carrier concentration. Nevertheless, this effect is less noticeable at lower temperatures.

As the temperature exceeds room temperature, the diffused drain current rises, leading to a decrease in mobility and further deterioration of the drift current. With an increase in V_{DS}, more charge carriers attempt to cross the narrow channel. However, beyond a specific threshold, the drain current reaches saturation, even as the drain voltage continues to increase.

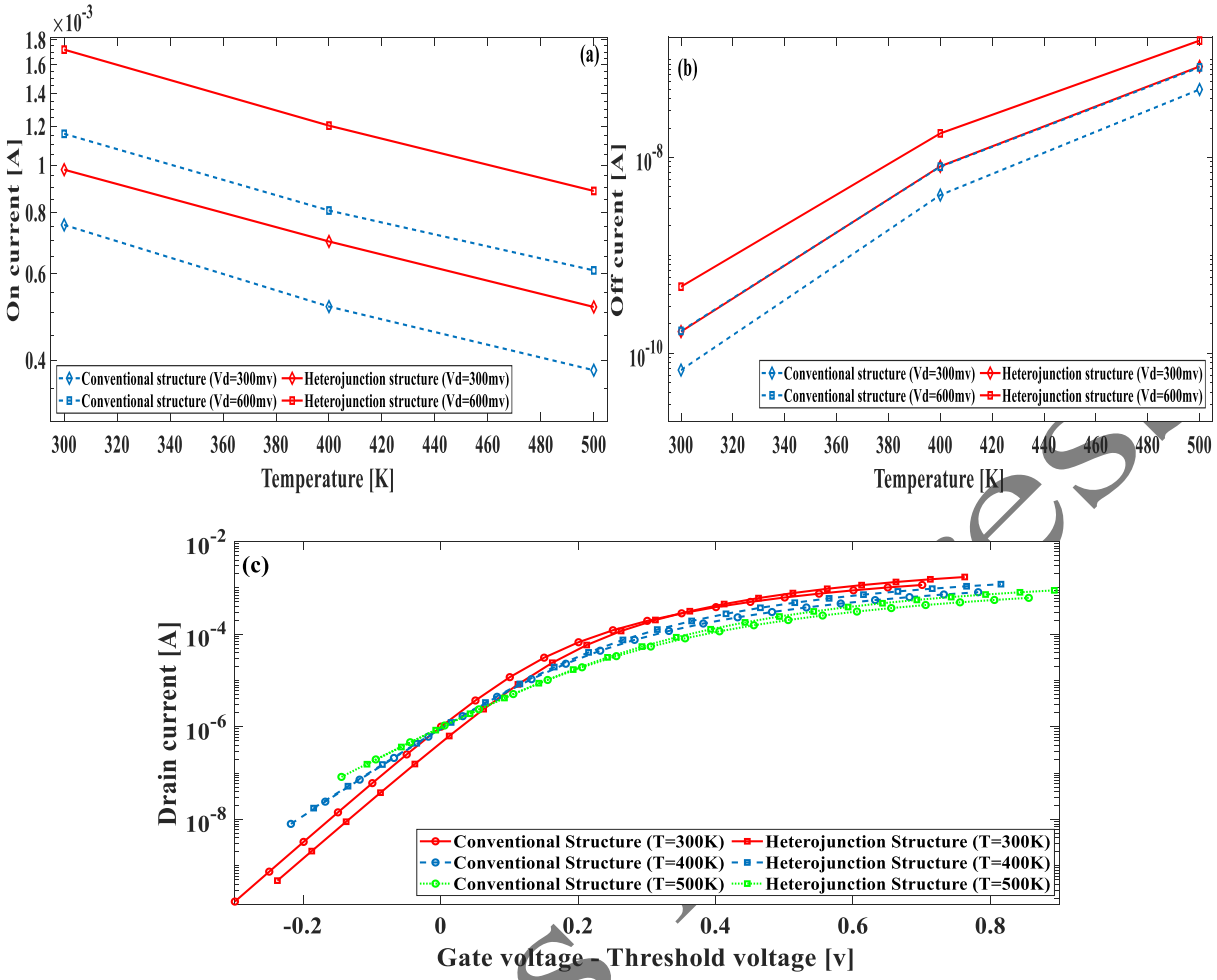


Fig. 8. (a) I_{ON} ratio under versus different temperatures, (b) I_{OFF} ratio under versus different temperatures, (c) Drain current of the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET under versus different temperatures in logarithmic scale

Table 4: Compration of electrical charactrize in 300 K

Vth(v)	Ion(A)	Ioff(A)	Reff
0 · 299	$1 \cdot 18 * 10^{-3}$	$169 * 10^{-12}$	**CDWN**
0 · 237	$1 \cdot 71 * 10^{-3}$	$479 * 10^{-12}$	**HDWNs**
0 · 440	$1 \cdot 81 * 10^{-5}$	$82 \cdot 41 * 10^{-12}$	**[23]**
0 · 251	$7 \cdot 71 * 10^{-4}$	$2 \cdot 8e * 10^{-12}$	**[24]**
0 · 239	$1 \cdot 02 * 10^{-4}$	$65 \cdot 3 * 10^{-12}$	**[32]**

This saturation phenomenon can be attributed to strain engineering and the heterojunction structure, both of which enhance carrier transport efficiency by facilitating the movement of additional carriers toward the drain side. On the other hand, a heterojunction structure provides several advantages over homojunctions, including enhanced carrier mobility, improved alignment of bandgaps, reduced leakage currents, and more effective confinement of carriers. The curve distinctly demonstrates that the drain current is significantly more pronounced for the Heterojunction DW GAA NS FET compared to its Conventional DW GAA NS FET counterparts, showcasing the benefits of utilizing a heterojunction structure in semiconductor devices.

With an increase in temperature, there is a notable rise in the OFF-state leakage current (I_{OFF}), whereas I_{ON} experiences only slight variations. This increase in I_{OFF} is attributed to temperature-dependent factors, such as diffusion current and Shockley-Read-Hall (SRH) recombination. It's observed that as temperature increases, the threshold voltage (V_{TH}) decreases. However, in structures lacking doping and featuring dual wires in the channel regions, ionized impurity scattering exerts significant control over mobility, in addition to lattice scattering.

Table 3 displays the threshold voltage values, I_{ON} and I_{OFF} determined from the $I-V$ characteristics of the mentioned devices. The threshold voltage is defined as the gate voltage at which the drain current reaches 1.0 μA (with various V_{GS} ranging from 0 to 1 V and V_{DS} set at 0 · 6V). Notably, the Heterojunction DW GAA NS FET demonstrates a lower threshold voltage compared to both the Conventional DW NS FET. Additionally, in Table 3, you can observe the ON and OFF state currents for all

structures at different temperatures (300K, 400K, and 500K). It becomes evident that the Heterojunction DW GAA NS FET offers higher ON current and a reduced OFF current. Both the ON and OFF state currents for these structures are illustrated in Fig. 8. The I_{ON} and I_{OFF} ratio is a crucial criterion for integrated circuits (ICs) and $CMOS$ technology, especially in low-power applications prioritizing high-speed operation. The Heterojunction DW GAA NS FET provides more space at the source-channel for carriers to drift when the transistor is in the ON state. This enhanced carrier velocity in the source and the effective channel width results in a larger ON current. Moreover, the conduction band offset energy leads to electrons gaining more kinetic energy, contributing to higher I_{ON} values. Consequently, the Heterojunction DW GAA NS FET demonstrates favorable switching characteristics, with significantly higher I_{ON} ratios (approximately 44%, 48% and 45%) compared to the Conventional DW GAA NS FET at various temperatures (300K, 400K and 500K). Furthermore, Table 4 provides a comparison of the electrical parameters influencing the Nanosheet FET with those from other sources.

3.2 AC Analysis

Temperature are critical parameters that significantly impact the analog/RF performance of semiconductor FET devices, making its selection a crucial aspect for specific applications. This section explores the influence of temperature on the analog/RF performance of vertically stacked silicon nanosheet FETs. The effect of changes in gate overdrive voltage on transconductance (g_m) at different temperatures (300K, 400K, and 500K) is illustrated in Fig. 9.

Transconductance, denoted as gm and calculated using the formula $g_m = \partial I_{DS}/\partial V_{GS}$ is directly obtained from Fig. 6. We examine the transconductance (g_m) characteristics of the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET at various V_{GS} and $V_{DS} = 0 \cdot 6\text{V}$, considering the source-relaxed SiGe/channel-strained Si heterointerface.

As the gate overdrive voltage increases beyond $0 \cdot 25V$, we observe a continuous rise in the transconductance of both devices, owing to the simultaneous increase in the drain currents. A higher gm in a device indicates improved transport efficiency within the channel, greater voltage gain for analog applications, and enhanced overall device performance. As illustrated in Fig. 9, the transconductance of the Heterojunction structures surpasses that of the Conventional structures.

Gate capacitance (C_{GG}) directly affects the gate voltage's ability to regulate charge carrier density in the channel Variations in drain current displace charge carriers within the channel, thereby influencing current flow and causing changes in transconductance. The improvement in transconductance of the Heterojunction DW GAA NS FET can be attributed to increased electron velocity, which enhances carrier mobility and reduces channel resistance.

In Fig. 10, we observe the variation of the total gate capacitance (C_{GG}) with respect to the gate voltage (V_G). The overall performance of these devices is significantly influenced by the total gate capacitance, which can be enhanced by reducing C_{GG}. In heterojunction-strained structures, C_{GG} is influenced by two primary factors: reducing the barrier between the source and the channel, and the accumulation of charges near the hetero-interface. In both structural configurations, capacitance increases as V_{GS} rises, resulting in extended propagation delay and reduced circuit performance, leading to slower switching speeds.

Nevertheless, a source heterojunction-strained channel exhibits greater capacitance due to an expanded parasitic capacitance area. Notably, at different temperatures (300K, 400K, 500K), the gate capacitance value for the Heterojunction DW GAA NS FET consistently exceeds that of the Conventional DW GAA NS FET.

The device's cut-off frequency (F_T) is influenced by both transconductance (g_m) and total gate capacitance (C_{GG}). In Fig. 11, the cut-off frequency characteristics at various temperatures (300K, 400K, and 500K) are shown for the Heterojunction DW GAA NS FET and the Conventional DW GAA NS FET. The calculation of the cut-off frequency follows the formula $F_T = g_m/2\pi C_{GG}$. Additionally, when the drain voltage increases, the device gains higher mobility, resulting in an increased transconductance. It is widely acknowledged that higher transconductance leads to higher cut-off frequencies. The results unequivocally show that the Heterojunction DW GAA NS FET outperforms the Conventional DW GAA NS FET in terms of cut-off frequency (F_T). This enhanced performance is attributed to superior gate control and increased transconductance. Optimizing these factors is essential for improving high-frequency device performance, especially in high-speed applications. The cut-off frequencies for the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET are summarized in Fig. 10 when $V_{GS} = 0 \cdot 8V$ and $V_{DS} = 0 \cdot 6V$.

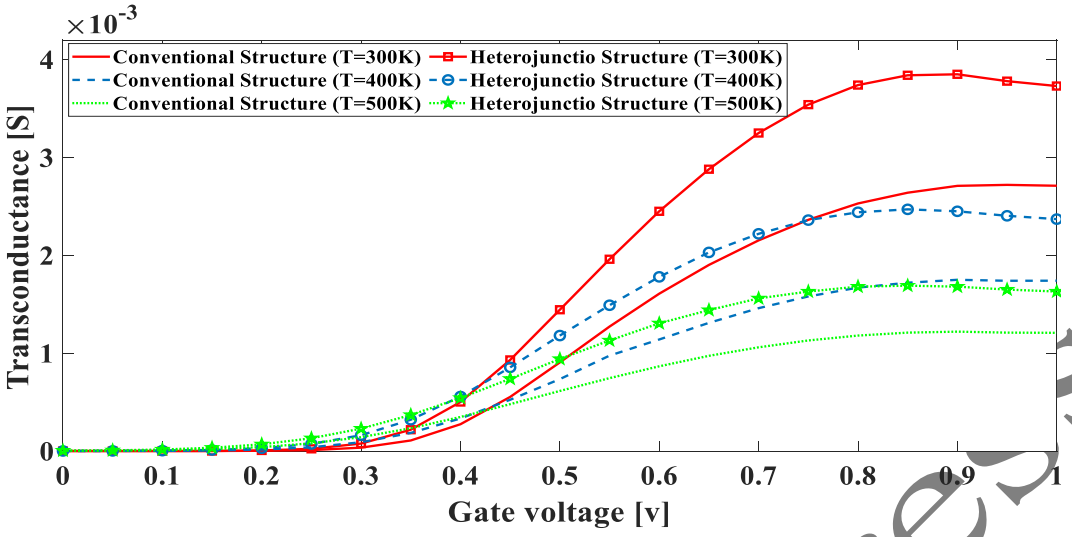


Fig. 9. Transconductance (gm) characteristics of the Heterojunction GAA NS FET and Conventional GAA NS FET under under versus different temperatures on V_{GS} and $V_{DS} = 0 \cdot 6V$

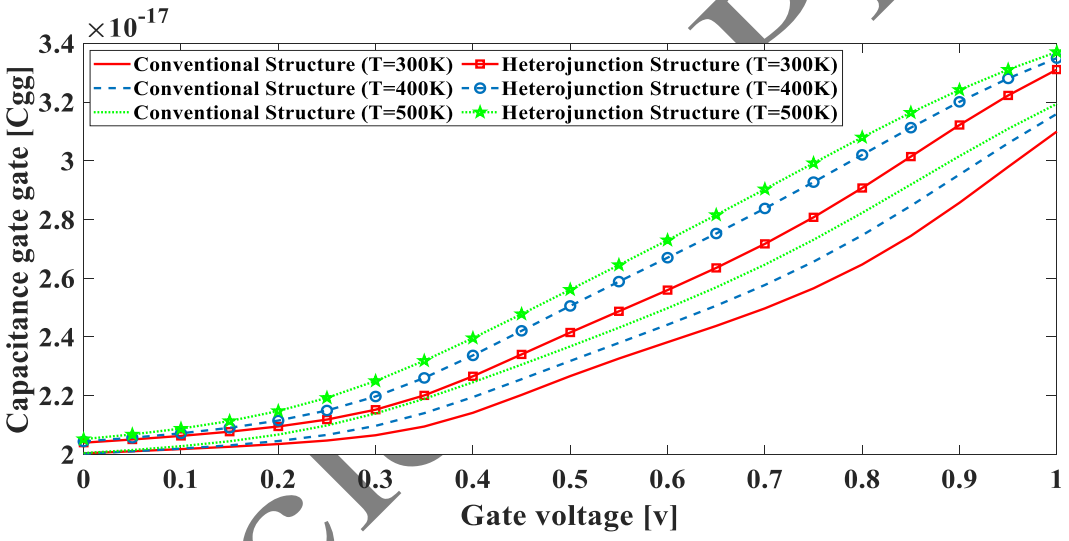
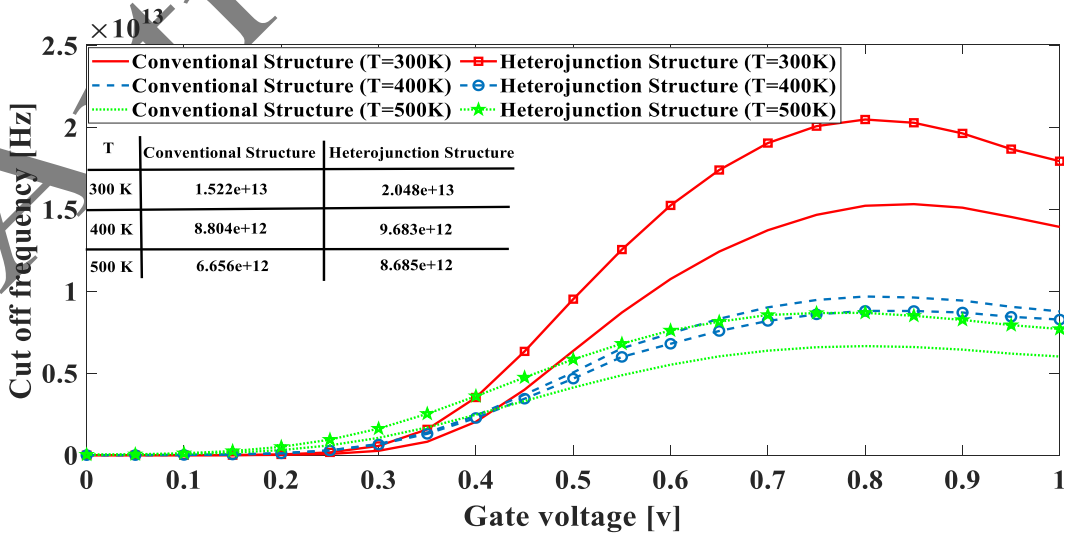


Fig. 10. The total gate capacitance with ac frequency=1MHz under various V_{GS} and $V_{DS} = 0 \cdot 6V$



T	Conventional Structure	Heterojunction Structure
300 K	1.522e+13	2.048e+13
400 K	8.804e+12	9.683e+12
500 K	6.656e+12	8.685e+12

Fig. 11. Cut-off frequency characteristics of the Heterojunction DW GAA NS FET and Conventional DW GAA NS FET under various V_{GS} and $V_{DS} = 0 \cdot 6V$

4. Conclusion

We conducted a comprehensive analysis of different device performance parameters for the of vertically stacked Heterojunction DW GAA NS FET and vertically stacked Conventional DW GAA NS FET devices. By simulating 3D Nanosheet Gate-All-Around transistor and introducing dual wires (DW) at the leftmost and rightmost ends of the main channel, we observed that in the OFF state, the channel experienced more pronounced carrier depletion. The impact of temperature variations on the AC and RF/analog performance of the devices was analyzed in detail, revealing that a lower temperature (300K) is preferable for achieving good performance characteristics. The ON-state current within the framework of the density gradient model in Heterojunction DW GAA NS FET amounted to nearly 40% of the ON-state current in conventional structures across different temperatures (300K, 400K, and 500K) and increased significantly. To sum up, our analysis showcased enhanced characteristics in the Heterojunction DW GAA Nanosheet FET compared to the Conventional DW GAA Nanosheet FET. Consequently, the Heterojunction DW GAA Nanosheet FET exhibits potential as a high-speed device for downscaled applications.

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