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Research note

The effect of annealing temperature on the characterization and electrical characteristics of NiO/PVC gate dielectric

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Abstract

The thickness of silicon oxide gate dielectric for field effect transistors is 1 to 2 nm. Therefore, reducing the thickness of gate to 1 nm for future products will increase the tunelling and leakage currents. The hybrid nano composites are good candidates as dielectric gates with high dielectric constant, wide band gap, and in thermal equilibrium in contact with silicon substrate. In the present work, we synthesized NiO/PVC hybrids as suitable dielectric materials by sol-gel method and tried to test the loss weight of samples against heat by using the thermogravimetric analysis (TGA) and its derivative. To measure the mobility, dielectric constant and conductivity of the samples at different annealing temperatures, we used A132GPS to calculate the activation energy in the logarithmic diagram in terms of temperature inverse. Results show that NiO/PVC:2 has less leakage current due to higher dielectric constant. The behavior of these samples is roughly the same rise up to 400 K. Differences between samples occur at higher temperatures so that the NiO/PVC:2 sample has a higher mobility at temperatures above 400 K**.**

Keywords: MOSFET nanotransistors, gate dielectric, NiO:PVC hybrid nanocomposite and sol gel method

For full article, refer to the Persian section